WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit including a plurality of standard cells which are arranged adjacent to each other in a cell row and composed of a plurality of MOS transistors, each standard cell of said cell row being provided with at least one first contact region through which at least one of said MOS transistors is electrically connected to a power potential, at least one second contact region through which at least one of said MOS transistors is electrically connected to a ground potential and first and second substrate regions located in upper and lower sides of the standard cell,

wherein said first substrate region is provided with at least one contact region through which said first substrate is electrically connected to said power potential while said second substrate region is provided with at least one contact region through which said second substrate is electrically connected to said ground potential,

wherein said first substrate region of said each standard cell is joined to the first substrate region of an adjacent cell of said cell row located adjacent to said each standard cell in order to form a first continuous region extending along said cell row in parallel while the second substrate region of said each standard cell is joined to the second substrate region of said adjacent cell in order to form a second continuous region extending along said cell row in parallel,

wherein said first contact region of said each standard cell is located beyond the boundary line between said each standard cell and said adjacent cell and shared by said each standard cell and said adjacent cell to function also as the first contact region of said adjacent cell,

wherein said at least one contact region of said first substrate region of said each standard cell is located to be inwardly displaced from the centers of said first substrate region in the longitudinal direction at the location where said

first substrate region has a minimum width and functions also as said first contact region of said each standard cell, and

wherein said at least one contact region of said second substrate region of said each standard cell is located to be inwardly displaced from the centers of said second substrate region in the longitudinal direction at the location where said second substrate region has a minimum width and functions also as said second contact region of said each standard cell.

2. The semiconductor integrated circuit as claimed in claim 1 wherein there is a vacant area where no functional cell is arranged in said cell row.

3. The semiconductor integrated circuit as claimed in claim 2 wherein said vacant area is padded with an inoperative cell which causes no operation.

4. The semiconductor integrated circuit as claimed in claim 3 wherein said inoperative cell is provided with a substrate region and a contact region.

5. The semiconductor integrated circuit as claimed in claim 1 wherein the widths of said first and second substrate regions have widths narrower than that as required for forming contact regions thereon under constraints determined by manufacture processes.

6. The semiconductor integrated circuit as claimed in claim 1 wherein the perimeters of said contact regions of said first and second substrate regions are displaced from the center positions of said first and second substrate regions by an interval no narrower than one half of a minimum allowable interval for complying with mask design rules.

7. The semiconductor integrated circuit as claimed in claim 1 wherein said contact regions of said first and second substrate

regions are located inwardly displaced from the inner perimeters of said first and second substrate regions at the location where the substrate regions 7 and 8 have minimum widths.

8. A semiconductor integrated circuit including a plurality of standard cells which are arranged adjacent to each other in a cell row and composed of a plurality of MOS transistors,

each standard cell of said cell row being provided with at least one first contact region through which at least one of said MOS transistors is electrically connected to a power potential, at least one second contact region through which at least one of said MOS transistors is electrically connected to a ground potential and first and second substrate regions located in upper and lower sides of the standard cell,

wherein said first substrate region of said each standard cell is joined to the first substrate region of an adjacent cell of said cell row located adjacent to said each standard cell within said each cell row in order to form a first substrate continuous region extending along said cell row in parallel while the second substrate region of said each standard cell is joined to the second substrate region of said adjacent cell in order to form a second substrate continuous region extending along said cell row in parallel,

wherein said first substrate continuous region is provided with a plurality of contact regions through which said first substrate is electrically connected to said power potential while said second substrate continuous region is provided with a plurality of contact regions through which said second substrate is electrically connected to said ground potential,

wherein said first substrate continuous region is provided with a plurality of expanded regions which are extended inwardly toward said standard cells in the longitudinal direction at the location, and

wherein said contact regions of said first substrate continuous region are located in said expanded regions.

9. A semiconductor integrated circuit including a plurality of standard cells which are arranged adjacent to each other in a cell row and composed of a plurality of MOS transistors,

each standard cell of said cell row being provided with at least one first contact region through which at least one of said MOS transistors is electrically connected to a power potential, at least one second contact region through which at least one of said MOS transistors is electrically connected to a ground potential and first and second substrate regions located in upper and lower sides of the standard cell,

wherein said first substrate region of said each standard cell is joined to the first substrate region of an adjacent cell of said cell row located adjacent to said each standard cell within said each cell row in order to form a first substrate continuous region extending along said cell row in parallel while the second substrate region of said each standard cell is joined to the second substrate region of said adjacent cell in order to form a second substrate continuous region extending along said cell row in parallel,

wherein said first substrate continuous region is provided with a plurality of contact regions through which said first substrate is electrically connected to said power potential while said second substrate continuous region is provided with a plurality of contact regions through which said second substrate is electrically connected to said ground potential,

wherein said first substrate continuous region is provided with a plurality of expanded regions which are extended inwardly toward said standard cells in the longitudinal direction at the location, and

wherein said expanded regions are formed in spaces which said standard cell can afford.

10. The semiconductor integrated circuit as claimed in claim 9 wherein said contact regions of said first substrate continuous region are located in said expanded regions.